OPEN ACCESS
Journal of Circuits, Systems, and Computers
Vol. 31, No. 18 (2022) 2240003 (25 pages)
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DOI: 10.1142/S0218126622400035

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Response of Commercial P-Channel Power VDMOS Transistors to Ionizing Irradiation and Bias Temperature Stress*,†

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*This paper was recommended by Regional Editor Zoran Stamenkovic.
†Extended paper from MIEL 2021 Conference to Journal of Circuits, Systems, and Computers.[1]
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Received 27 February 2022
Accepted 22 April 2022
Published 7 July 2022

In this paper, the effects of successively applied static/pulsed negative bias temperature (NBT) stress and irradiation on commercial p-channel power vertical double-diffused metal-oxide semiconductor (VDMOS) transistors are investigated. To further illustrate the impacts of these stresses on the power devices, the relative contributions of gate oxide charge (N_{ot}) and interface traps (N_{it}) to threshold voltage shifts are shown and studied. It was shown that when irradiation without gate voltage is used, the duration of the pre-irradiation static NBT stress has a slightly larger effect on the radiation response of power VDMOS transistors. Regarding the fact that the investigated components are more likely to function in the dynamic mode than the static mode in practice, additional analysis was focused on the results obtained during the pulsed NBT stress after irradiation. For the components subjected to the pulsed NBT stress after the irradiation, the effects of N_{ot} neutralization and N_{it} passivation (usually related to annealing) are more enhanced than the components subjected to the static NBT stress, because only a high temperature is applied during the pulse-off state. It was observed that in devices previously irradiated with gate voltage applied, the decrease of threshold voltage shift is significantly greater during the pulsed NBT stress than during the static NBT stress.

Keywords: VDMOS transistors; irradiation; pulsed NBT stress; static NBT stress.

1. Introduction

The aim of this paper is to perform an analysis of the power vertical double-diffused metal-oxide semiconductor (VDMOS) transistors threshold voltage behavior during the pulsed and static negative bias temperature (NBT) stress after the irradiation. Also, an analysis of contributions of gate oxide charge and interface traps to threshold voltage shifts, as well as their relative contributions, was performed in the paper. These analyses, in addition to analyses during the irradiation after the static NBT stress (lasted 1 h and 1 week),[1] can contribute to comprehensive understanding of the threshold voltage behavior of VDMOS transistors in the harsh environment.

First of all, it should be mentioned that power MOS field effect transistors (MOSFETs) are highly specialized transistors that are designed to operate at high power levels. Various different designs were used in the early stages of manufacturing, but VDMOS components became the dominant type.[2,3] In addition to having a high drain to source breakdown voltage, they are capable of carrying large drain currents. VDMOS power transistor's unique characteristics permitted their widespread use in commercial and special purpose applications. These components are extensively used for power regulation in household electrical devices, industrial and military electronics.[2,3] Also, their use is common in switching power sources and audio amplifiers, as well as in complex systems representing both primary and optional equipment in the automobile industry.[2,3] Power transistors may be exposed to more demanding working conditions and/or stress in these and numerous similar applications. This is the reason for the growth of interest in determining the impacts on functioning under specific settings and environments, as well

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as their reliability.[1–19] These studies have highlighted the impact of high electric fields,[4–6] irradiation[7–9,17,18] and accelerated high temperature bias stresses.[10–16] It should be mentioned that ionizing radiation could damage the power VDMOS transistors by causing considerable changes in their electrical characteristics, and consequently, their parameters.[7,8,18] Specifically, during irradiation, transconductance decreases, leakage current increases, breakdown voltage decreases and most notably, threshold voltage (V_T) changes.[18–21] However, the device's design-determined parameters must remain stable, i.e., move within the required boundaries, during a particular period of use in the specified environment. If any of the parameters deviates from the defined range, a device failure could occur. A classification can be made using many criteria,[3] and selecting highly reliable components for usage in a radiation environment involves the reliability check technique. Besides, standard reliability testing for these components includes burn-in tests, which incorporates the application of bias and elevated temperatures.[1,10,11,21]

Moreover, negative bias temperature instability (NBTI) effects may appear during testing and, in some situations, during normal operation of power VDMOS transistors. These effects are more prominent in p-channel components and occur at temperatures ranging from 100 to 250°C and gate oxide electric fields of 2–6 MV/cm.[12,22,23] In addition, VDMOS transistors can be NBT stressed and irradiated simultaneously or successively,[1,24–28] as well as in combination with other forms of stressing.[11,29] Specifically, p-channel power VDMOS transistors are exposed to space radiation (which is a constant threat) as a component of the electronic equipment used in satellites. A total dose of up to 10 kGy (SiO_2) could be stored if they are established in high orbits, while in lower orbits, total doses could be significantly less — about 100 Gy (SiO_2) and even less.[30] Simultaneously, using these transistors without applying appropriate cooling can result in an increase in their operating temperature. Thus, operation at maximum power or at elevated temperatures can result in the activation of mechanisms that cause NBTI. As a result, it is evident that investigating the processes behind both NBTI and irradiation effects is required. These mechanisms are triggered by electrochemical reactions that create and/or activate defects in the gate oxide and at the gate oxide-silicon interface. Under the effect of irradiation and applied negative gate bias at elevated temperatures — NBT stress, electrochemical processes form gate oxide (N_{ot}) and interface (N_{it}) traps. Therefore, the increase, in absolute value, of the threshold voltage is due to both the gate oxide charge and interface traps.

NBTI has become a progressively more relevant reliability concern, as the oxide thickness reduces with each technology generation. Despite the fact that device dimensions are shrinking, examinations of reliability difficulties in ultra-thick gate oxides are still of interest due to the widespread use of MOS technology in power components. With this in mind, previous studies[12,31,32] were focused on NBTI in p-channel power VDMOS transistors. Due to its improved switching characteristics, which allow operation in the megahertz frequency range, this type of transistor is a

suitable device for use in high-frequency switching power supplies.[33] The VDMOS transistors reliability has been studied extensively under a variety of stress circumstances, including irradiation, high electric field, hot carrier injection, unclamped inductive switching, NBTI, NBTI under low magnetic field, as well as combined NBTI and irradiation.[11,14,29,33–36]

Measurements,[31,33] mechanisms of degradation,[12,15,32,33,35,36] effect on device lifetime,[34] relationship between the recoverable and permanent components of degradation in components subjected to the static and pulsed NBT stress[15,32,33,35] were investigated. Also, the effects of consecutive irradiation and the NBT stress on threshold voltage were addressed in previous papers.[24–28] Despite many years of researching stresses which significantly initiate MOS transistor parameters modifications, the mechanisms that lead to changes in their electrical parameters have not been fully elucidated. Additionally, it is the fact that electronic components are installed in electronic systems that are difficult to diagnose and service, resulting in greater repair and maintenance expenses. As a result, numerous researchers continue to conduct studies on diverse impacts. In this study, the effects of consecutive irradiation, and two types of NBT stresses (static and pulsed) in p-channel power VDMOS transistors are described.

Namely, it is important to examine the constant NBT stress in order to understand the degradation mechanisms and changes over the long period of using devices. On the other hand, components are switched on and off alternately in a variety of applications. As such, it is necessary to investigate this mode of operation. When the pulsed stress is applied, the gate bias switches between "high" (pulse-on state) and "low" (pulse-off state) voltage levels. Due to the fact that components are partly strained, the resulting degradation is less severe than when the static NBT stress is applied, due to a recovery effect. The degradation that occurs during the fraction of period corresponding to the pulse-on state of the gate stress voltage is neutralized and/or annealed during the fraction of period corresponding to the pulse-off state.[27,36,37] Also, the impact of irradiation before and after the NBT stress was analyzed. It is known that when transistors are operated in a radiation environment at increased temperatures, they are exposed to both the NBT stress and the action of the ionizing radiation. On the other hand, backup components are exposed only to the ionizing radiation and later, they can be exposed to NBT during the operation.

To further understand the impacts of these stresses on investigated transistors, the contributions of gate oxide charge ($\Delta V_{\rm ot}$) and interface traps ($\Delta V_{\rm it}$) to threshold voltage shifts ($\Delta V_{\rm T}$) are considered and explained in this research. Additionally, the behaviors of relative contributions[38] of $\Delta V_{\rm ot}$ and $\Delta V_{\rm it}$ to $\Delta V_{\rm T}$ may be important for supplementary analyses. The further investigation results of threshold voltage instabilities derived from the experiments on commercially used p-channel power VDMOS transistors IRF9520 subjected to the irradiation and static as well as pulsed NBT stress have been presented in a comprehensive discussion. The relative contributions of $\Delta V_{\rm ot}$ and $\Delta V_{\rm it}$ to $\Delta V_{\rm T}$ during the NBT stress and irradiation

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(which occur one after the other) are presented in this study, too. The analysis of these relative contributions may be of importance in further elucidating the electrochemical processes that occur in components, as this could be valuable for their reliable operation in electronic equipment.

2. Experimental Details

2.1. *Experimental conditions and equipment*

In this experiment, p-channel power VDMOS transistors were used as examined components. These components are commercially available under the code IRF9520. Several fundamental properties of these components include the fact that they are made using the standard poly-Si technology and have a gate thickness of approximately 100 nm. The highest current that can be applied to these transistors is 6.8 A, while the threshold voltages measured prior to the experiments were around $V_{T0} = -3.6$ V. The components are packaged in a TO-220 plastic cases, contain 1650 cells and have a hexagonal configuration.

All experiments in this study were conducted by a previously developed technique based on a switching circuit that has been established to provide a suitable trade-off between the NBT stress and measurement demands in power VDMOS transistors.[31] The technique has been validated using the NBTI testing in a variety of experiments.[15,32,33,39] As it could be observed in Fig. 1, the whole setup is divided into three parts.

The first (marked with the number 1) is responsible for providing the static ($V_G = -45$ V) or pulsed ($V_G = -45$ V, $f = 10$ kHz and DTC = 50%) gate voltage. For obtaining the proper gate voltage, a signal generator and power supply

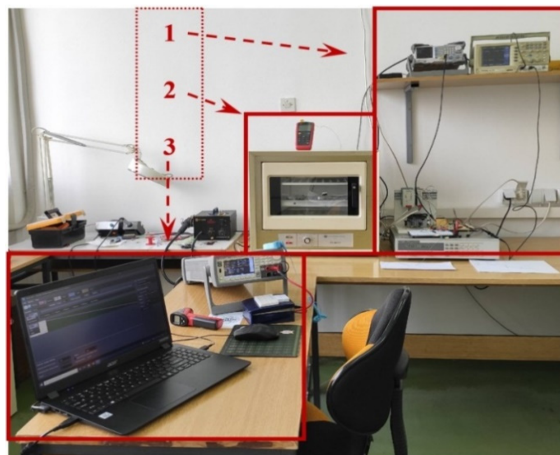

Fig. 1. Experimental setup in the laboratory: 1, stress setup; 2, heating chamber; and 3, measurement setup.

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are necessary. To track the pulsed signal sent to tested component, the oscilloscope is placed at the input of the circuit. The second part of setup (marked with the number 2) represents the heating chamber. Using this chamber, the temperature of $T = 175^{\circ}$C could be established. The third part of experimental setup (marked with the number 3) includes the source measurement unit (SMU) Keysight B2901A is accessed by the computer. To perform I-V measurements with this technique, the stress voltage, which was static or pulsed, must be removed from the device under test, and the threshold voltage is then estimated from the measured transfer characteristic.

Apart from the NBT stress, the irradiation process was carried out. Throughout the irradiation, a gate voltage of -10 V was provided to transistors of previously chosen groups, while the gate voltage was not applied to the remaining groups. All samples were irradiated by Co-60 γ-ray source with dose rate of 0.5 Gy(SiO_2)/min. It should be noted that MOS devices integrated into medical or nuclear power equipment may also be exposed to similar ionizing radiation dose rates.[40,41] The whole radiation procedure was performed at the Metrological Laboratory of the Institute for Nuclear Sciences in Vinča, Serbia.

The experiment, performed by previously explained equipment, consists of two parts. All steps of both parts of the experiment are depicted in Fig. 2.

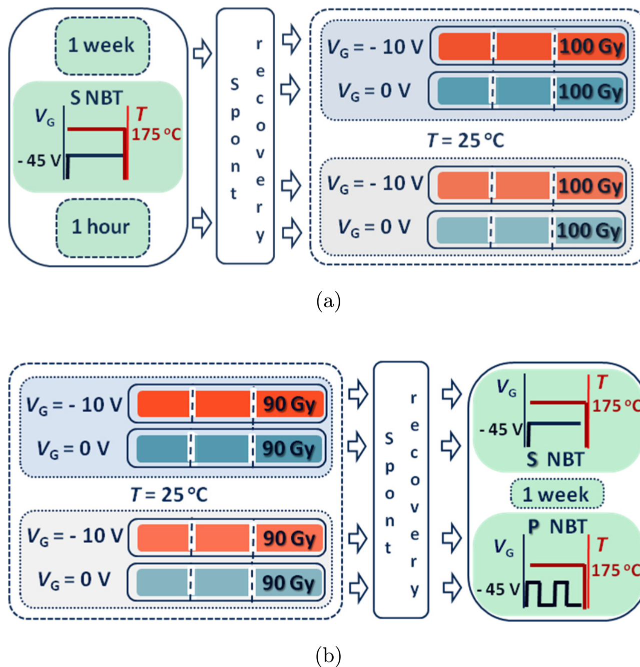

Fig. 2. Schematic presentation of the experimental conditions for (a) the first and (b) the second part of the experiment.

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In the first part of the experiment [Fig. 2(a)], the components were NBT stressed and after that irradiated. Throughout the NBT stress, the temperature was maintained at 175°C, the gate was biased to −45 V, and the source and drain terminals were grounded for all transistors. The one group of components was subjected to the NBT stress for 168 h (1 week), whereas another group was subjected to the NBT stress only for 1 h. These time intervals of 1 h and 1 week correlate to the ending of the first and second phases of threshold voltage shifts (which follow the well-known t^n power low) during the NBT stress.[1,16,34,42] After a spontaneous recovery at room temperature, components were irradiated up to 100 Gy. Before the irradiation, components from each group were divided into two subgroups. The components from the first two subgroups, one of each group, were irradiated with a gate voltage of −10 V, while the components from the other two subgroups were irradiated without a gate voltage (with all terminals connected to the ground).

The second part of the experiment had different arrangement [Fig. 2(b)]. First, the process of irradiation was performed, and the components were divided into two groups, depending on the applied polarization, −10 and 0 V, and irradiated up to 90 Gy. After the spontaneous recovery, the last part of the experiment was the NBT stress during 1 week. Before the NBT stress, components from each group were divided into two subgroups. The components from the first two subgroups, one of each group, were the static NBT stressed (S NBT) for one week, while components from the other two subgroups were the pulsed NBT stressed (P NBT).

The transfer characteristics are measured in order to investigate the effects of applied stresses on transistors. Using SMU Keysight B2901A, the transfer characteristics of VDMOS transistors ($I_D = f(V_G)$) were analyzed following the previously established periods of the NBT stress and gamma-irradiation, at temperature of 25°C.

2.2. *Experimental results*

The subthreshold characteristics of fresh, NBT-stressed and irradiated components under $V_G = -10$ V for 1 week and 1 h are shown in Figs. 3(a) and 3(b), respectively. It is visible that the negative bias temperature stress shifted the subthreshold characteristics in the direction of greater negative values along the V_G axis, and that this shift is more significant when NBT stressing was performed for 1 week. During the following irradiation, characteristics of all transistors exhibited a considerable shift toward more negative values along the V_G axis.

On the other hand, the subthreshold characteristics of fresh, irradiated components under $V_G = -10$ V and subsequently NBT static and pulsed stressed for 1 week are shown in Figs. 4(a) and 4(b), respectively. Also, the performed irradiation moved the characteristics of all transistors toward more negative values along the V_G axis. It can be seen that the NBT stress performed after the irradiation shifted the subthreshold characteristics in the direction of less negative values along the V_G axis. This shift is more significant when the pulsed NBT stressing was applied.

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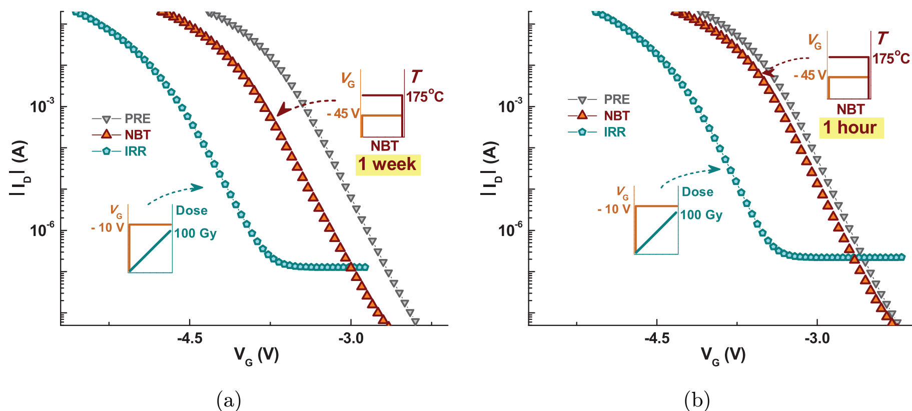

Fig. 3. Representative subthreshold characteristics of fresh and irradiated (with gate polarization) components previously NBT stressed during (a) 1 week and (b) 1 h.

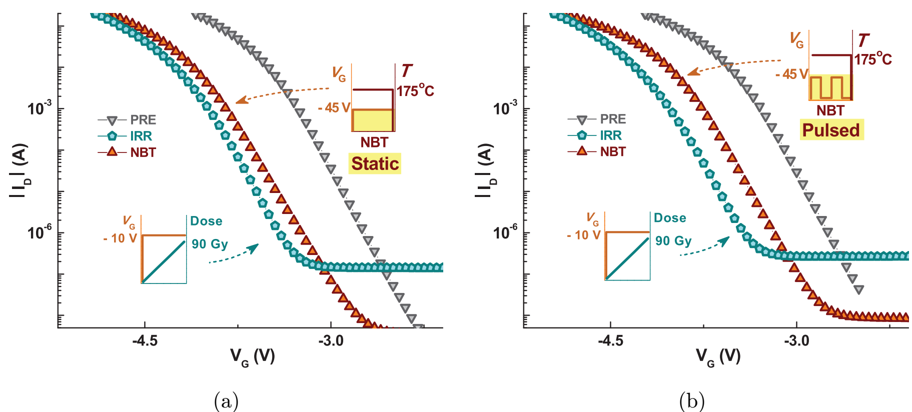

Fig. 4. Representative subthreshold characteristics of fresh, irradiated (with gate polarization) and 168 h NBT stressed components by (a) static and (b) pulsed stress.

The applied measurement technique enables full-range measurement of the transfer I-V characteristics, which may be used to extract the threshold voltage. In this way, it might provide a better understanding of the impacts of successive irradiation and static/pulsed NBT stresses.

3. Analysis of Obtained Results

3.1. *Threshold voltage shifts*

The threshold voltage was determined using transfer characteristics as the cross section of the V_G axis and the line extrapolating the linear region of (sqrt I_D)-V_G curves.

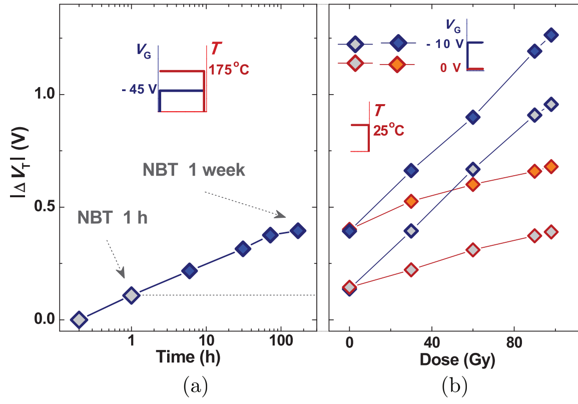

Fig. 5. The threshold voltage shift induced by (a) NBT stress and (b) irradiation (without and with gate polarization) for different time (1 h and 1 week) NBT stressed components.

The threshold voltage shifts ΔV_T [determined during the first part of the experiment — Fig. 2(a)] are reported in Fig. 5. The NBT stress resulted in considerable negative threshold voltage shifts for 1 week compared to 1 h [Fig. 5(a)]. The spontaneous recovery, which followed at room temperature, did not result in significant variations of the threshold voltage shifts, while irradiation [Fig. 5(b)] resulted in a further negative ΔV_T. This additional shift was significantly more evident in components irradiated with gate voltage of −10 V than that achieved in components irradiated without a gate voltage applied. It should be noted that the variations in the occurred and initiated processes during the first (1 h) and second (1 week) phases of NBT stress may result in minor differences in the threshold voltage response during the following irradiation.

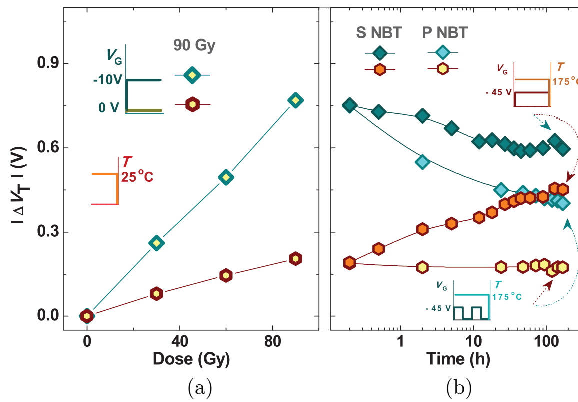

Fig. 6. The threshold voltage shift induced (a) by irradiation (without and with gate polarization) and (b) by static and pulsed NBT stress.

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The threshold voltage shifts [determined during the second part of the experiment — Fig. 2(b)] are reported in Fig. 6. It can be seen that the irradiation of fresh components [Fig. 6(a)] resulted in a significant negative ΔV_T, which was more evident in components irradiated with the gate voltage of -10 V than that achieved in components irradiated without a gate voltage applied. The spontaneous recovery, which followed at room temperature, resulted in a slight reduction of the threshold voltage shifts in all components. On the other hand, the following NBT stress resulted in different ΔV_T which strongly depended on applied polarization during irradiation, and on stressing types — static or pulsed [Fig. 6(b)].

As illustrated in Fig. 6(b), the static NBT stress resulted in a large decrease of ΔV_T for components irradiated with the negative gate voltage applied. For components irradiated without gate polarization applied, ΔV_T resulted in the significant increase. It should be noted that the pulsed NBT stress [Fig. 6(b)] resulted in a greater reduction of ΔV_T for components irradiated with the negative gate voltage applied than the static NBT. For components irradiated without the gate voltage applied, pulsed NBT stress resulted in small changes of ΔV_T.

It is known that the change in the threshold voltage shift occurs as a result of positive oxide trapped charge in the gate oxide — N_{ot} and traps generated at the SiO_2-Si interface — N_{it}. Due to that fact, it is necessary to estimate their particular contribution to the change of the threshold voltage. This assessment was made using the well-established subthreshold mid-gap technique.[43]

3.2. *Contributions of oxide-trapped charge and interface traps to V_T shift*

Regarding the first part of the experiment [Fig. 2(a)], the threshold voltage shifts obtained, as well as the contributions of gate oxide charge and interface traps to this

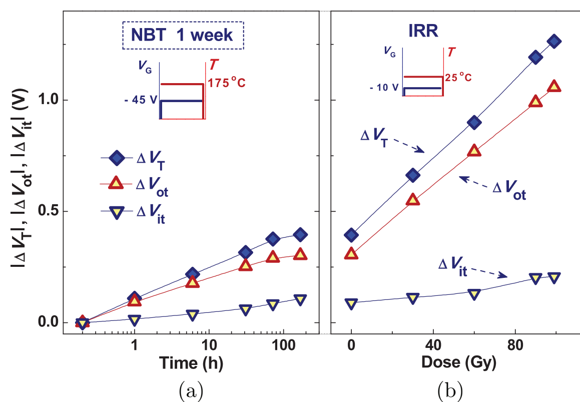

Fig. 7. The threshold voltage shift, contributions of gate oxide charge and interface traps during: (a) static NBT stress and (b) irradiation (with gate polarization), for components NBT stressed during 1 week.

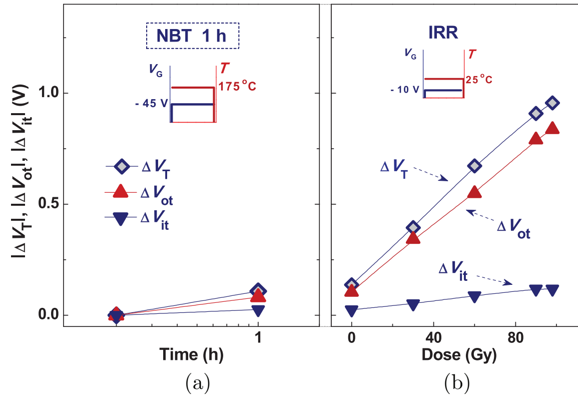

Fig. 8. The threshold voltage shift, contributions of gate oxide charge and interface traps during: (a) static NBT stress and (b) irradiation (with gate polarization), for components NBT stressed during 1 h.

shift, during the NBT stress and irradiation (with the gate negatively polarized), for transistors NBT stressed for 1 week and 1 h, respectively, are shown in Figs. 7 and 8. As seen in these figures, during both stress and irradiation, ΔV_{ot} contributes more to ΔV_{T} than ΔV_{it}, what is in accordance with the representative subthreshold characteristics behavior presented in Fig. 3.

During NBT, in the first phase which lasts for 1 h [Fig. 8(a)], the parameter n in the power low t^n is temperature and bias dependent and ranges between 0.4 and 1.14. In the second phase of the NBT stress which lasts for 1 week [Fig. 7(a)], the parameter n is temperature and bias independent and has a constant value of approximately 0.25. This power low dependence of ΔV_{T} during the stress may imply that the underlying processes are diffusion-controlled.[1,22,42] It is worth noting that near the end of the second phase of the stress, the contribution of ΔV_{ot} is slightly reduced, while the contribution of ΔV_{it} is reinforced.

Throughout the irradiation ΔV_{T} of all transistors considerably increased [Figs. 7(b) and 8(b)] for all components for which the static NBT stress lasted for an hour as well as for 1 week. It is obvious that the contributions of the gate oxide charge and interface traps to threshold voltage shifts grow in the absolute value with the increasing total dose.[1] Variations in the stress-induced processes in the first and second phases can explain modest differences in the ΔV_{T} rise (in absolute value). A slightly pronounced increase in ΔV_{T} was detected during the irradiation for components stressed with the static NBT for 1 week, not only in the absolute value, but also in proportion to the value following the prior stress.[1] This is most likely the result of electrochemical reactions that happened during the stress and are associated with interface traps, hydrogen-associated species, holes and oxide defects.[28]

Namely, during the irradiation, pairs of electrons and holes are formed in the gate oxide, and while the majority of electrons are ejected, the majority of holes are captured in oxide defects or at the interface. A certain disparity in the activation of

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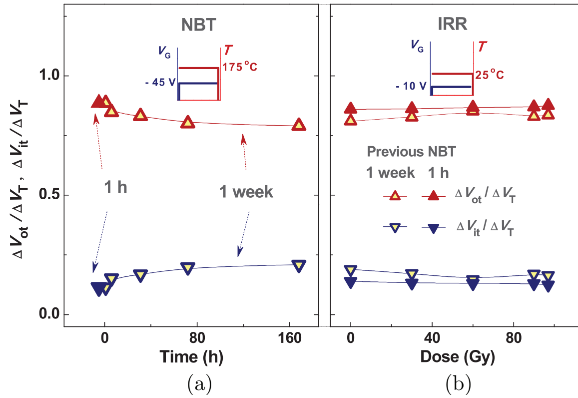


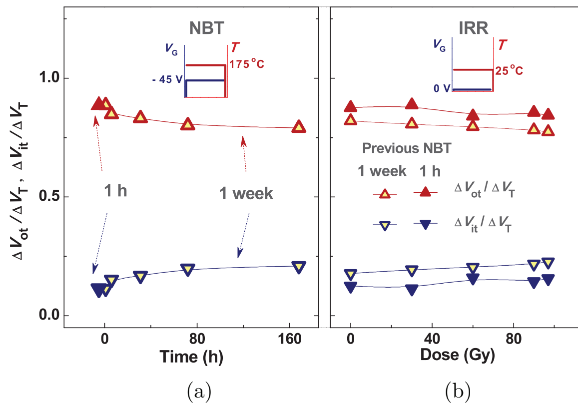
(a) (b)

Fig. 9. Contributions of gate oxide charge and interface traps relative to the threshold voltage shift during: (a) static NBT stress and (b) irradiation with gate polarization.

defects precursors during NBT stress could result in observed differences during irradiation.

To further elucidate the effects of the static NBT stress and subsequent irradiation, with and without negative gate bias, the relative contributions of ΔV_{ot} and ΔV_{it} to the ΔV_{T} are shown in Figs. 9 and 10, respectively, for transistors NBT stressed for 1 week and 1 h.

As illustrated in Figs. 9(a) and 10(a), the relative contribution of the oxide-trapped charge ($\Delta V_{\mathrm{ot}}/\Delta V_{\mathrm{T}}$) reduces continually under the static NBT stress, but the relative contribution of the interface-trapped charge ($\Delta V_{\mathrm{it}}/\Delta V_{\mathrm{T}}$) increases continuously. These tendencies are significantly more prominent during the initial hours of the stress, although they moderate slightly toward the end of the week. After the first



(a) (b)

Fig. 10. Contributions of gate oxide charge and interface traps relative to the threshold voltage shift during: (a) static NBT stress and (b) irradiation without gate polarization.

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hour, ΔV_{ot} contributed less than 90%, less than 85% after 30 h and slightly less than 80% in the final part of the week. In contrast, in the first hour, ΔV_{it} contributed slightly more than 10%, after 30 h, slightly more than 15% and at the end of the week, slightly more than 20%. These variations in the relative contributions could be as a result of the local electric field reducing along the SiO_2-Si interface. Specifically, when the oxide-trapped charge grows, the local electric field reduces, resulting in a decreased buildup of N_{ot} and a corresponding drop in the contribution $\Delta V_{\text{ot}}/\Delta V_{\text{T}}$. Simultaneously, the oxide-trapped charge can be transformed into interface traps, resulting in a buildup of N_{it}.

Table 1 summarizes the contributions of the oxide-trapped charge and the interface traps during irradiation without and with negative gate bias in components previously NBT stressed for 1 week and 1 h.[1] As illustrated in Fig. 9(b), no significant changes in the contributions of the oxide-trapped charge and the interface traps can be observed during irradiation with applied $V_{\text{G}} = -10\,\text{V}$.

Specifically, for components stressed with NBT for 1 week, the values for $\Delta V_{\text{ot}}/\Delta V_{\text{T}}$ are in the range 0.819–0.836, but for components stressed for 1 h, the values are in the range 0.861–0.876, and as can be seen, these values are extremely close. Values $\Delta V_{\text{it}}/\Delta V_{\text{T}}$ which correspond to components that have been stressed for 1 week are slightly higher (0.181–0.164) than those of the devices that have been stressed for 1 h (0.139–0.124). Additionally, as seen in Fig. 9(b), the ΔV_{ot} contribution to ΔV_{T} is more pronounced (and thus ΔV_{it} is less pronounced) in the components that were previously stressed for 1 h. Presumably, when devices are stressed for an hour, there are more precursors accessible for the formation of the oxide-trapped charge during the irradiation.

As seen in Fig. 10(b), under irradiation without gate voltage applied, both subgroups of components exhibit a drop in oxide-trapped charge contribution at a similar rate. Consequently, there is an increase in the contribution of N_{it}, which occurs at a similar rate in both subgroups of components.

Specifically, even when the gate is not biased, there is a slight electric field in the oxide due to the small work-function difference between the poly-Si gate and the n-bulk of a p-channel VDMOS transistor, which can affect the holes generated by the irradiation.[1,44,45] Holes and positive oxide charge are drawn toward the interface

Table 1. Relative contributions of V_{ot} and of V_{it} to V_{T} during the irradiation with $V_{\text{G}} = -10\,\text{V}$ and $V_{\text{G}} = 0\,\text{V}$.

Previous NBT stress	Irradiation			
	$V_{\text{G}} = -10\,\text{V}$		$V_{\text{G}} = 0\,\text{V}$	
Time	$\Delta V_{\text{ot}}/\Delta V_{\text{T}}$	$\Delta V_{\text{it}}/\Delta V_{\text{T}}$	$\Delta V_{\text{ot}}/\Delta V_{\text{T}}$	$\Delta V_{\text{it}}/\Delta V_{\text{T}}$
1 week	0.819–0.836	0.181–0.164	0.821–0.774	0.179–0.226
1 h	0.861–0.876	0.139–0.124	0.875–0.843	0.125–0.157

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(through hole trapping). The local electric field near the interface decreases as the oxide-trapped charge increases, and this effect is more noticeable when the gate voltage is not applied during irradiation. This is evident from the results reported in Table 1, where $\Delta V_{\mathrm{ot}}/\Delta V_{\mathrm{T}}$ values range between 0.821 and 0.774 for components stressed for 1 week and between 0.875 and 0.843 for devices stressed for 1 h. The values are higher for transistors that have been stressed for 1 h, which may be due to the increased availability of defects in the oxide that act as precursors for oxide-trapped charge.

Considering the contribution of interface traps, it can be noted that the values of $\Delta V_{\mathrm{it}}/\Delta V_{\mathrm{T}}$ are in the range 0.179–0.226 for components stressed for 1 week, but in the range 0.125–0.157 for components stressed for 1 h. Specifically, interface traps can be formed when released holes and hydrogen ions dissociate weak bonds at the interface.[46,47] The fraction of holes accessible for the dissociation of weak bonds in the oxide, as well as for the reactivity with hydrogen atoms (formation of ions) and the dissociation of weak bonds at the interface, is reduced for components stressed for 1 h, due to a more pronounced hole capture in the oxide.[1]

These subtle but noticeable changes may have an effect on the radiation response of embedded power transistors over the course of the satellite or electronic device long-term mission in a radiation environment. Hence, a full investigation and better understanding of the underlying mechanisms that occurred in components exposed not only to the radiation after NBT, but also exposed to NBT after the radiation, may be of high importance.

Regarding the second part of the experiment [Fig. 2(b)], the threshold voltage shift, contributions of gate oxide charge and interface traps during the irradiation up to 90 Gy (without and with gate polarization) and the NBT stress are presented in Figs. 11 and 12, respectively, for the static and pulsed stress. As seen in these figures, during both the irradiation and stress, ΔV_{ot} contributes more to ΔV_{T} than ΔV_{it},

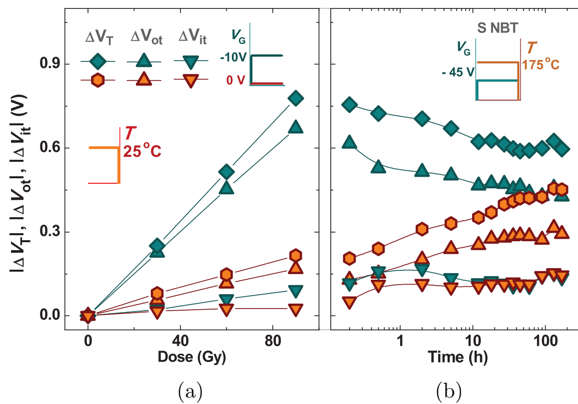

Fig. 11. The threshold voltage shift, contributions of gate oxide charge and interface traps during: (a) irradiation (without and with gate polarization) and (b) static NBT stress.

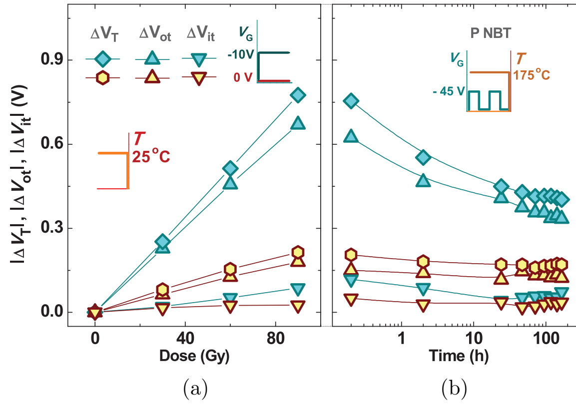

Fig. 12. The threshold voltage shift, contributions of gate oxide charge and interface traps during: (a) irradiation (without and with gate polarization) and (b) pulsed NBT stress.

what is in accordance with representative subthreshold characteristics behavior presented in Fig. 4.

The shift of V_T during the irradiation was significantly more evident in components irradiated with gate voltage of -10 V than achieved in components irradiated without a gate voltage applied [Figs. 11(a) and 12(a)]. These differences are explained by the electric-field dependency of irradiation effects.[48] Namely, when the negative bias is applied, electrons are eliminated via the semiconductor, because bulk is connected internally to the source, which is grounded during the irradiation. As can be observed, the values of ΔV_{ot} are much greater than those of ΔV_{it} at the end of the irradiation, and all changes are significantly lower in the absence of the gate bias. It is worth noting that after the spontaneous recovery there is only a slight decrease of ΔV_T. However, while the threshold voltage does not appear to vary considerably, the ΔV_{it} and ΔV_{ot} contributions have an obvious change. In both subgroups (with and without the gate voltage applied), after the spontaneous recovery, ΔV_{ot} decreased while ΔV_{it} increased. Namely, after the spontaneous recovery, the values of ΔV_{ot} were lower after the irradiation while the values of ΔV_{it} were higher. This could indicate that the electrochemical processes that occurred and triggered, may have the effect on the ΔV_T response during the subsequent NBT stress.

Although components irradiated after the NBT stress behave very similar to fresh components exposed to radiation, components subjected to NBT stress after radiation behave differently from fresh components. It is worth noting that electrochemical processes occurring during the NBT stress are actually different from the processes that occurred during the irradiation, although some of the associated processes can be represented by similar reactions.

In the case of components irradiated with negative polarization, the complete NBT phase [Fig. 11(b)] is characterized by a general decreasing trend of ΔV_{ot} values

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until the completion of the static NBT stress. On the other hand, in the case of components irradiated without polarization, through the whole NBT stress process, $\Delta V_{\rm ot}$ values increase. Considering the $\Delta V_{\rm it}$ values, it is obvious that for all components there is an increase in $\Delta V_{\rm it}$ values during the early part of the NBT stress followed by a modest decrease and then an increase to the end of the NBT stress, and this is more pronounced for components irradiated with the gate voltage applied.

It can be seen from Fig. 12(b) that final values of $\Delta V_{\rm ot}$ and $\Delta V_{\rm it}$ are lower than at the beginning of this stress until the completion of the pulsed NBT stress. The decreases are more pronounced in the components previously irradiated with the gate voltage applied due to significantly larger number of charged defects in the oxide and the charge captured at the interface traps. It is obvious that in both subgroups the values of $\Delta V_{\rm ot}$ are significantly higher than $\Delta V_{\rm it}$ values.

It is evident that two mechanisms could be responsible for the effects observed during the NBT stress after the irradiation. The first mechanism is related to activation of electrochemical reactions contributing to NBT instabilities, resulting in the additional oxide charge and interface trap formation. The second mechanism is associated to the annealing of irradiation-induced oxide charge due to implemented high temperature of 175°C and thermally activated processes.

Namely, during the NBT stress, interfacial weak Si-H bonds can be dissociated, thus creating interface traps,[22,38,49] while the buildup of oxide-trapped charge can be ascribed to hole capturing at the oxygen vacancy defects[12] and at the dangling bonds near the interface.[25] However, processes of $N_{\rm ot}$ transformations into the $N_{\rm it}$ may be pronounced in the case when there is a certain amount of $N_{\rm ot}$. Also, thermally supported processes (which are dominant during annealing) can come to the fore. Diffusion of hydrogen molecules from the high concentrations areas (in the oxide) to the low concentrations areas (near the interface) may occur and hydrogen molecules can be cracked at charged oxide traps, leading to decrease of $N_{\rm ot}$. Therefore, the effects of the oxide-trapped charge transformation into the interface traps and annealing are prevailing, during the static NBT, in components previously irradiated with the gate voltage applied. At the same time, as a result of transformation, there is a small increase of $N_{\rm it}$. On the other hand, in devices that had previously been irradiated without the gate polarization, the amount of radiation-induced defects was relatively low, whereas the number of defect precursors remained very high. As a result, the subsequent static NBT stress in this example was predominantly accompanied by an increased defect formation, resulting in an increase in oxide-trapped charge and interface traps.

At pulsed NBT stress (in the conducted experiment, the duty cycle was 50%), voltage and elevated temperature were applied during practically only half of the pulses, while only elevated temperature was applied in the other half of the pulses. Namely, in the case of pulsed stress conditions, the applied gate bias was alternated between the high and the low voltage levels. In fact, the bias was alternating between two states: pulse-on and pulse-off. This is the reason for significantly less degradation

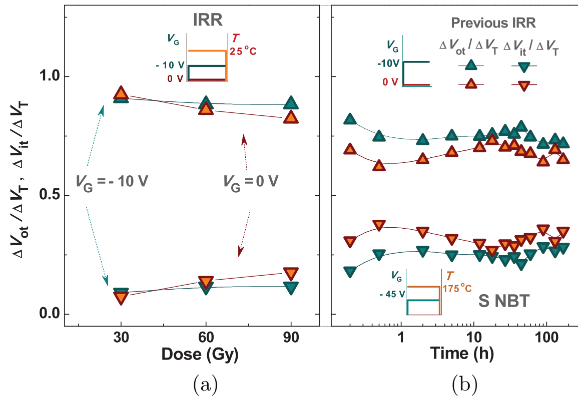

Fig. 13. Contributions of gate oxide charge and interface traps relative to the threshold voltage shift during: (a) irradiation (without and with gate polarization) and (b) static NBT stress.

in fresh components subjected to the static and pulsed NBT stress. Also, this is the reason for more pronounced annealing effects during the pulsed NBT stress in previously irradiated components [Fig. 12(b)], than it is caused under the static NBT stress [Fig. 11(b)].

In order to further elucidate the effects of the NBT stress after the irradiation (without and with the negative gate bias), the relative contributions of ΔV_{ot} and ΔV_{it} in the ΔV_{T} are shown in Figs. 13 and 14, for transistors stressed by the static and pulsed NBT stress, respectively.

As illustrated in Figs. 13(a) and 14(a), in all fresh components, the relative contribution of the oxide-trapped charge ($\Delta V_{\mathrm{ot}}/\Delta V_{\mathrm{T}}$) during the irradiation is somewhat higher than in previously NBT stressed components [Figs. 9(b) and 10(b)], and the relative contribution of the interface-trapped charge ($\Delta V_{\mathrm{it}}/\Delta V_{\mathrm{T}}$) is

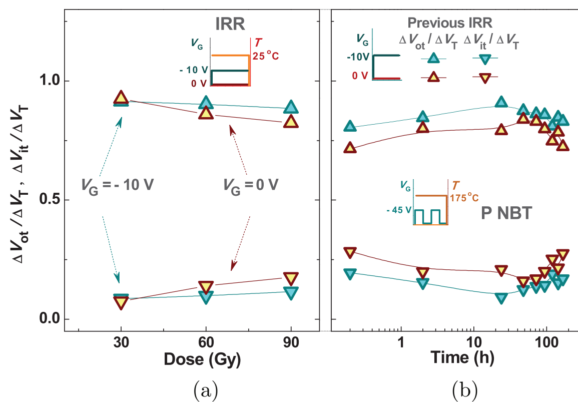

Fig. 14. Contributions of gate oxide charge and interface traps relative to the threshold voltage shift during: (a) irradiation (without and with gate polarization) and (b) pulsed NBT stress.

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somewhat lower. Also, it can be noticed that in components irradiated without the applied gate voltage, the contribution of the oxide-trapped charge noticeably reduces, and the contribution of the interface trapped charge increases. This tendency is in accordance with observed changes in previously NBT stressed components. For components irradiated with the applied gate voltage, there is no such noticeable tendency of the contribution of the oxide-trapped charge, as well as interface traps, during irradiation up to 90 Gy. Namely, for these components the relative contribution of $\Delta V_{\rm ot}$ is about 90% (0.91–0.88) while $\Delta V_{\rm it}$ is about 10% (0.09–0.12). On the other hand, for components irradiated without the applied gate voltage, $\Delta V_{\rm ot}/\Delta V_{\rm T}$ is in the range 90–80% (0.92–0.82), while $\Delta V_{\rm it}/\Delta V_{\rm T}$ is in the range 10–20% (0.08–0.18). As mentioned, these variations in relative contributions could be the result of a decrease in local electric field along the SiO_2-Si interface, which causes a reduced buildup of $N_{\rm ot}$.

Table 2 summarizes the contributions of the oxide-trapped charge and the interface traps during the static and pulsed NBT stress in components previously irradiated without and with applied negative gate bias. As illustrated in Fig. 13(b), during the applied static NBT stress, there is an initial decrease of $\Delta V_{\rm ot}/\Delta V_{\rm T}$ during first hours — 2 h for components irradiated with the applied gate voltage and 1 h for components irradiated without the applied voltage. This could be attributed to the pronounced effects of the $N_{\rm ot}$ transformation into the $N_{\rm it}$, and consequently, the observed $\Delta V_{\rm ot}$ decreases and $\Delta V_{\rm it}$ increases. Although this transformation is usually attributed to a later phase of NBT stress of fresh components,[50] probably it may occur in this initial phase because a certain amount of oxide-trapped charge is previously created during the irradiation. The initial decrease of $\Delta V_{\rm ot}$ is followed by the slight increase and some oscillations of $\Delta V_{\rm ot}/\Delta V_{\rm T}$ in the last part of static NBT stress.

Specifically, for components irradiated with the applied gate voltage these values for $\Delta V_{\rm ot}/\Delta V_{\rm T}$ are in the range 0.82–0.72, but for components irradiated without the applied gate voltage the values are in the range 0.73–0.62. The range is slightly larger for components irradiated without the gate voltage, and differences are more noticeable in the initial period. This initial somewhat noticeable decrease could be attributed to relatively more pronounced effects of the $N_{\rm ot}$ transformation into

Table 2. Relative contributions of $V_{\rm ot}$ and of $V_{\rm it}$ to V_T during the static and the pulsed NBT stress.

Previous irradiation	NBT stress for 1 week			
	Static		Pulsed	
V_G	$\Delta V_{\rm ot}/\Delta V_T$	$\Delta V_{\rm it}/\Delta V_T$	$\Delta V_{\rm ot}/\Delta V_T$	$\Delta V_{\rm it}/\Delta V_T$
−10 V	0.816–0.715	0.184–0.285	0.805–0.906	0.195–0.094
0 V	0.731–0.622	0.269–0.378	0.715–0.838	0.285–0.162

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the N_{it}. In the case of created N_{ot}, the effect of local electric field may have a more pronounced influence on relative changes of ΔV_{ot}. Corresponding values of $\Delta V_{\mathrm{it}}/\Delta V_{\mathrm{T}}$ for components that have been irradiated with the applied gate voltage are in the range 0.18–0.28, but for components irradiated without the applied gate voltage, the values are in the range 0.27–0.38. These values are in accordance with $\Delta V_{\mathrm{ot}}/\Delta V_{\mathrm{T}}$ values, as well as previously described and explained effects. It is obvious that values of $\Delta V_{\mathrm{it}}/\Delta V_{\mathrm{T}}$ are generally lower than $\Delta V_{\mathrm{ot}}/\Delta V_{\mathrm{T}}$, but in the initial part of the static NBT stress they are somewhat closer to each other. This indicates almost the same contributions of ΔV_{ot} and ΔV_{it} to ΔV_{T}, which is in accordance with the values presented in Fig. 11(b).

As seen in Fig. 14(b), under the pulsed NBT stress, in all components, $\Delta V_{\mathrm{ot}}/\Delta V_{\mathrm{T}}$ shows an initial increase followed by a decrease. The initial increase of $\Delta V_{\mathrm{ot}}/\Delta V_{\mathrm{T}}$, during the first part of the pulsed NBT stress, approximately 1 day for components irradiated with the applied gate voltage and approximately 2 days for components irradiated without the applied voltage, could be caused by a more pronounced reduction of oxide-trapped charge due to enhanced annealing effects in comparison to the static NBT. Namely, beside transformation, neutralization of positive oxide traps can be reinforced during the pulsed NBT stress. Throughout off-state (when only enhanced temperature is applied), thermally activated processes may come to the fore. Hydrogen molecules can diffuse toward the interface where their concentration is lower. They can be cracked at the oxide-trapped charge leading to neutralization of positive oxide traps, which is the most pronounced in the first part of the NBT stress after the irradiation, when still there is a high amount of oxide-trapped charge. The pronounced ΔV_{ot} decline contributes to a more noticeable decrease of ΔV_{T} [Fig. 12(b)] compared to the static NBT [Fig. 11(b)]. The initial increase of $\Delta V_{\mathrm{ot}}/\Delta V_{\mathrm{T}}$ is followed by a decrease [Fig. 14(b)], which indicates lowered ΔV_{ot} contribution to the ΔV_{T}. Namely, during the NBT stress after the irradiation, the amount of previously created oxide-trapped charge is reduced and thus the process of hydrogen molecules cracking is reduced in the later phase of NBT. Also observed initial decrease of ΔV_{it}, which is more noticeable in devices irradiated with the applied gate voltage [Fig. 12(b)], could be ascribed to the passivation of interface traps. Reduced ΔV_{it} contribution to the ΔV_{T} resulted in the reduction of $\Delta V_{\mathrm{it}}/\Delta V_{\mathrm{T}}$, as presented in Fig. 14(b). This passivation is related to electrochemical processes which also involve hydrogen species like the hydrogen molecule and very reactive hydrogen atom. In the later phase of NBT, interface traps available for the passivation are reduced, leading to an increase of relative contribution.

Specifically, for components irradiated with the applied gate voltage, these values for $\Delta V_{\mathrm{ot}}/\Delta V_T$ are in the range 0.81–0.91, but for components irradiated without the applied gate voltage the values are in the range 0.72–0.84. Corresponding values $\Delta V_{\mathrm{it}}/\Delta V_T$ for components that have been irradiated with the applied gate voltage are in the range 0.19–0.09, but for components irradiated without the applied gate voltage the values are in the range 0.28–0.16. It can be seen that the values of

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$\Delta V_{\text{ot}}/\Delta V_T$ are higher in the case of the static NBT stress, indicating a more pronounced neutralization of oxide-trapped charge created during the previous irradiation (during the pulse-off state) and less pronounced creation of oxide-trapped charge due to the processes related to the static NBT (during the pulse-on state). Also, the values $\Delta V_{\text{ot}}/\Delta V_T$ are higher in devices previously irradiated with the applied bias because the amount of irradiation-induced oxide-trapped charge was substantially greater, and its contribution was actually more pronounced.

It is important to mention that in the absence of a radiation environment the degradation under the pulsed NBT stress is less severe than under the static NBT stress. The reason for this is a recovery effect because a portion of the degradation caused by the pulse-on state of the gate stress voltage is neutralized and/or annealed during the pulse-off state of the gate stress voltage. However, during the pulsed NBT stress after irradiation under bias applied, the threshold voltage decrease is greater during the static NBT stress. Namely, the reduction of defects created during the irradiation was greater during the pulsed-off state because of enhanced annealing effects. Regarding the p-channel power, VDMOS transistors are more likely to function in the dynamic mode than the static mode in practice, this may have an implication on the operation of these components in harsh environment conditions. Consequently, the observed changes may have an effect on the radiation response of embedded power transistors over the course of the satellite or electronic device mission in a radiation environment. Thus, a complete investigation and greater understanding of the underlying mechanisms may be beneficial for elucidating the effects that occur in the devices during the irradiation and when they are exposed to an environment that can create NBT instabilities.

4. Conclusions

In commercial p-channel power VDMOS transistors, the effects of successively applied static/pulsed NBT stress and radiation were evaluated. To further understand the impacts of 1 h and 1 week of the applied NBT stress on the irradiation of these components, as well as the irradiation on subsequent static and pulsed NBT stress, the relative contributions of gate oxide charge and interface traps to threshold voltage shifts are presented and analyzed in this paper.

Although the radiation tolerance appears to be similar in situations after 1 h and after 1 week of the applied static NBT stress, the diverse contributions of ΔV_{ot} and ΔV_{it} suggest that possible changes in electrochemical processes (occurred during the first and the second phases) may have an effect on the radiation response, and therefore, on the device reliability. It was shown that when the irradiation without the gate voltage is used, the duration of the pre-irradiation NBT stress has a greater effect on the radiation response of power VDMOS transistors than when the gate voltage is used.

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Regarding the fact that the investigated components are more likely to function in the dynamic than in the static mode in practice, the additional analysis was focused on the results obtained during the pulsed NBT stress after the irradiation. For the transistors subjected to the pulsed NBT stress after the irradiation, the effects of the oxide-trapped charge neutralization and the interface traps passivation are more enhanced than those for transistors subjected to the static NBT stress, because only high temperature is applied during the pulse-off state. It was revealed that the decrease of ΔV_T is much higher, in devices previously irradiated with the gate voltage applied, in the case of the pulsed than in the case of the static NBT stress. Also, the oxide-trapped charge contribution to the V_T is significantly greater in the case of the pulsed NBT stress. This suggests that, in addition to transformation, the neutralization of positive oxide traps can be enhanced during the pulsed NBT stress because throughout off-state (when only elevated temperature is applied) thermally activated processes may come to the fore.

These findings indicate that a complete investigation and a greater understanding of the underlying mechanisms may be beneficial for elucidating the effects that occur in the devices during the irradiation and when they are exposed to an environment that can create NBT instabilities.

Acknowledgments

This work was supported by the European Union's Horizon 2020 research and innovation program (Grant No. 857558 — ELICSIR) and the Ministry of Education, Science and Technology Development of the Republic of Serbia under the Grant No. 451-03-9/2021-14/200102. The authors would like to thank the staff of the Laboratory of Radiation and Environmental Protection, Institute "Vinča", for experimental support. Passed away academician Ninoslav D. Stojadinović, with his knowledge during many years of cooperation, made significant contribution to this paper.

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